confusing and/or lack clear antecedent basis. By this response, each of the noted points of indefiniteness has been appropriately addressed. Specifically, non-sequiturs eliminated and confusing and/or vague language deleted in favor of language believed to recite the invention with the degree of precision and particularity required by the statute. Therefore, it is respectfully urged that the rejection be withdrawn.

REJECTION OF CLAIMS UNDER 35 U.S.C. §§ 102 AND 103

Claims 1 and 12 stand rejected under 35 U.S.C. § 102(e) as being anticipated by Adams.

Claims 2, 3, 13, 14 and 31-33 stand rejected under 35 U.S.C. § 103 as being unpatentable over Adams. The Examiner recognizes that certain elements are not disclosed in Adams, but asserts that the use of output buffers and read registers is well known and use of more than one array would have been obvious in order to test more than one array for faulty elements.

Claims 4 and 5 stand rejected under 35 U.S.C. § 103 as being unpatentable over Adams in view of Getzlaff and further in view of An.

Claim 10 stands rejected under 35 U.S.C. § 103 as being unpatentable over Adams in view of Getzlaff et al.

Adams discloses a defective cell repairing circuit using a data compressor for programming a defective address.

The compressor of Adams compares a test data pattern from a test pattern generator with a data pattern read from the selected memory cells, and generates a one-bit pass/fail signal in accordance with the result of comparison. Adams' memory device is not a synchronous type. In addition, the pass/fail signal of Adams is used internally for storing a defective address in the failed address register.

In the present invention, data are subject to logical operation for compression, and no comparison is carried out.

Getzlaff discloses a set of submultiplexers for selecting a predetermined number of bits located beginning at an arbitrary position in consecutively arranged data bits. A multiplier includes an AND gate provided for each input, and an OR gate receiving outputs of AND gates. In accordance with an output of a multiplexer control, one AND gate is enabled on each submultiplexer and the output of the enabled AND gate is outputted through an OR gate. In Getzlaff, only selection of a predetermined number of bits from a plurality of data bits is carried out, and no compression is carried out. Regarding the arrangement of claim 10, Getzlaff discloses 4 AND gates in Figs. 5A which arrangement is substantially different from the present invention. Thus, the present invention is significantly different from Getzlaff.

An discloses a DRAM having a precharge circuit provided for each bit line pair for precharging a corresponding bit line pair to a predetermined precharge level. However, An fails to show the

precharging of other elements such as a row decoder. In the present invention, the precharging is carried out for all the elements in the corresponding bank. In other words, the "precharging" means "inactivation" in the present invention.

Again, it is important to note that primary reference Adams is not a synchronous semiconductor memory device.

To expedite prosecution, claims 1-5, 10 and 12 are amended to recite subject matter which is clearly not disclosed or suggested by the applied references. More specifically, claim 1 is amended to delineate that the read mode command is "incorporated in synchronization with the clock signal" and that the compression means carries out a prescribed "logical" operation. Claims 2-5 are similarly amended.

Claim 10 is amended to delineate that each gate of each n-channel insulated gate type field effect transistor receives each respective data, the plurality of n-channel insulated gate type field effect transistors are connected between a first signal line and a first potential node, a second wired circuit is provided separately from the first wired circuit and has a plurality of p-channel insulated gate type field effect transistors each having a gate receiving each respective data read by the read means with the plurality of p-channel insulated gate type field effect transistors connected between a second signal line and a second potential node, and logic means is coupled to receive signals on the first and second signal lines.

Claim 12 is amended to clarify that the data output means externally supplies received data in synchronization with the clock signal.

It is believed that claims 1-5 and 12, as amended, are patentable over the applied references and it is respectfully requested that they be allowed.

Claim 9 stands rejected under 35 U.S.C. § 103 as being unpatentable over Ueoka in view of An. Ueoka is held to teach all the elements except precharging means. An is held to teach use of precharge means for precharging memory arrays bank by bank.

Ueoka discloses a semiconductor memory device having a plurality of blocks of memory cells and having data written or read on a block basis in a normal mode of operation. The Examiner asserts that the pulsed clock signal is applied in Ueoka. However, in Ueoka, strobing of the write enable signal /WE and address signal bits is not carried out by the pulsed clock signal. The block address bits of Ueoka are applied only to the block selecting circuit for activating a block controller. A "synchronous DRAM" of the present invention incorporates external signals such as an address signal and a control signal in synchronization with the clock signal. Ueoka's memory device is <u>not</u> a synchronous memory device.

In Ueoka, all the blocks are selected to be accessed in a test mode of operation. Ueoka describes the dynamic stress test on column 7, lines 20 through 34. In this test mode of operation, a

group of memory cells is selected in each memory block, and data is simultaneously written into the selected memory cells in the respective memory blocks. However, the block of Ueoka is substantially different from the bank of the present invention. In Ueoka, only a block designated by a block address is activated in a normal mode of operation, and another block cannot be activated at the same time.

In the present invention, in a normal mode of operation, the banks cannot be activated at the same timing, but the banks can be activated at different timings even if a bank is being activated, as shown in Fig. 16 of the present application.

Again, it is important to note that primary reference Ueoka is not a synchronous semiconductor memory device.

To expedite prosecution, claim 9 is amended to delineate that a synchronous semiconductor memory device incorporates external signals including address signals and control signals in synchronization with a clock signal. Each of a plurality of banks includes means for selecting a memory cell designated by an address signal incorporated in synchronization with the clock signal. In addition, a first activation means is responsive to a bank address signal designating a bank incorporated in synchronization with the clock signal for activating a bank designated by the bank address signal, independently of the states of activation and precharging of remaining banks in a normal mode of operation.

It is believed that claim 9 as amended, is patentable over the applied references and it is respectfully requested that they be allowed.

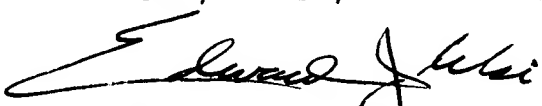
CONCLUSION

Accordingly, it is urged that the application, as now amended, overcomes the rejection of record and is in condition for allowance. Entry of the amendment and favorable reconsideration of this application, as amended, are respectfully requested. If there are any outstanding issues which might be resolved by an interview or an Examiner's amendment, Examiner is requested to call Applicants' attorney at the telephone number shown below.

To the extent necessary, a petition for an extension of time under 37 C.F.R. 1.136 is hereby made. Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account 12-2237 and please credit any excess fees to such deposit account.

Respectfully submitted,

LOWE, PRICE, LEBLANC & BECKER



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